Designing neuromorphic circuits with memristive technologies

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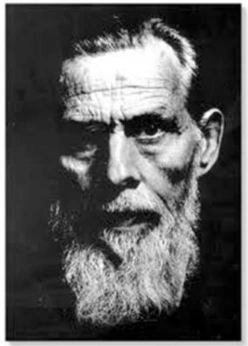
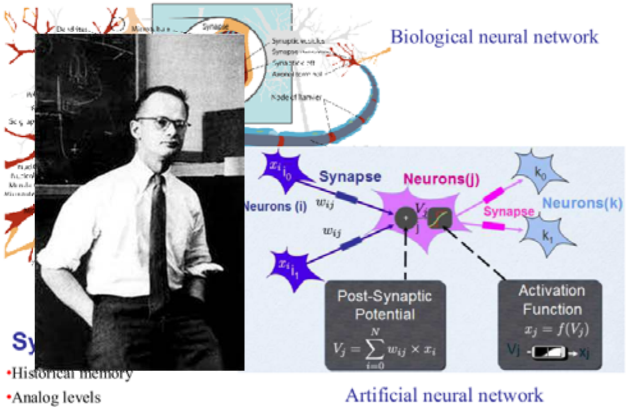
Outline

- Intro: a brief look back at neuromorphic engineering
  - Introducing the STDP learning rule
- Memristors as a synapse-like devices
  - Introducing the device synapticity
- Designing synaptic arrays
  - Impact of memristive technologies on circuits
- And now, what do we do?
  - A glimpse into possible applications, can those things really learn?
- Summary

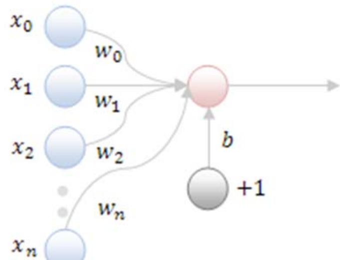
A brief history of neuro-engineering

1943 – Mc Culloch & Pitts
The formal neuron

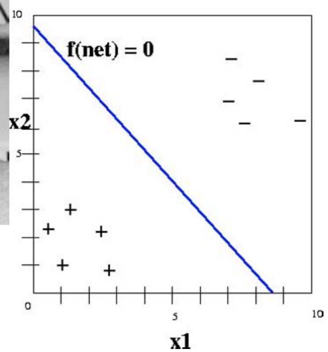




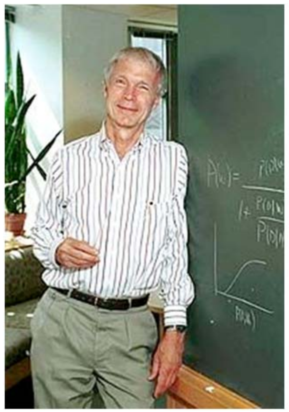
1958 – F. Rosenblatt
The perceptron

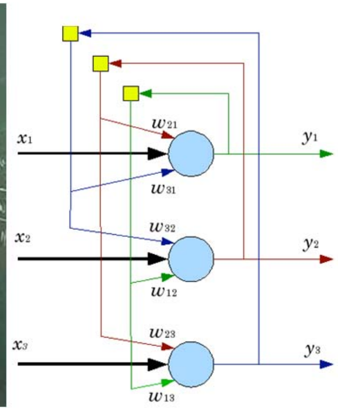


1970 – Minsky & Pappert
Xor is the problem!



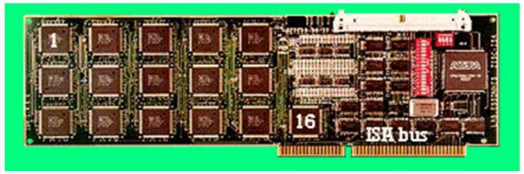
1981 – J.J. Hopfield
Physics to the rescue





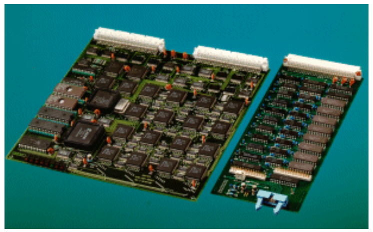
1980’s Neurocomputers Galore!...

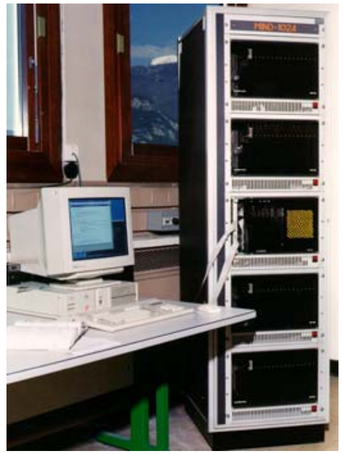
- Siemens : MA-16 Chips (SYNAPSE-1 Machine)
  - Synapse-1, neurocomputer with 8xM-A16 chips
  - Synapse3-PC, PCI board with 2xMA-16 (1.28 Gpcs)
- Adaptive Solutions : CNAPS
  - SIMD // machine based on a 64 PE chip.



- IBM : ZISC
  - Vector classifier engine

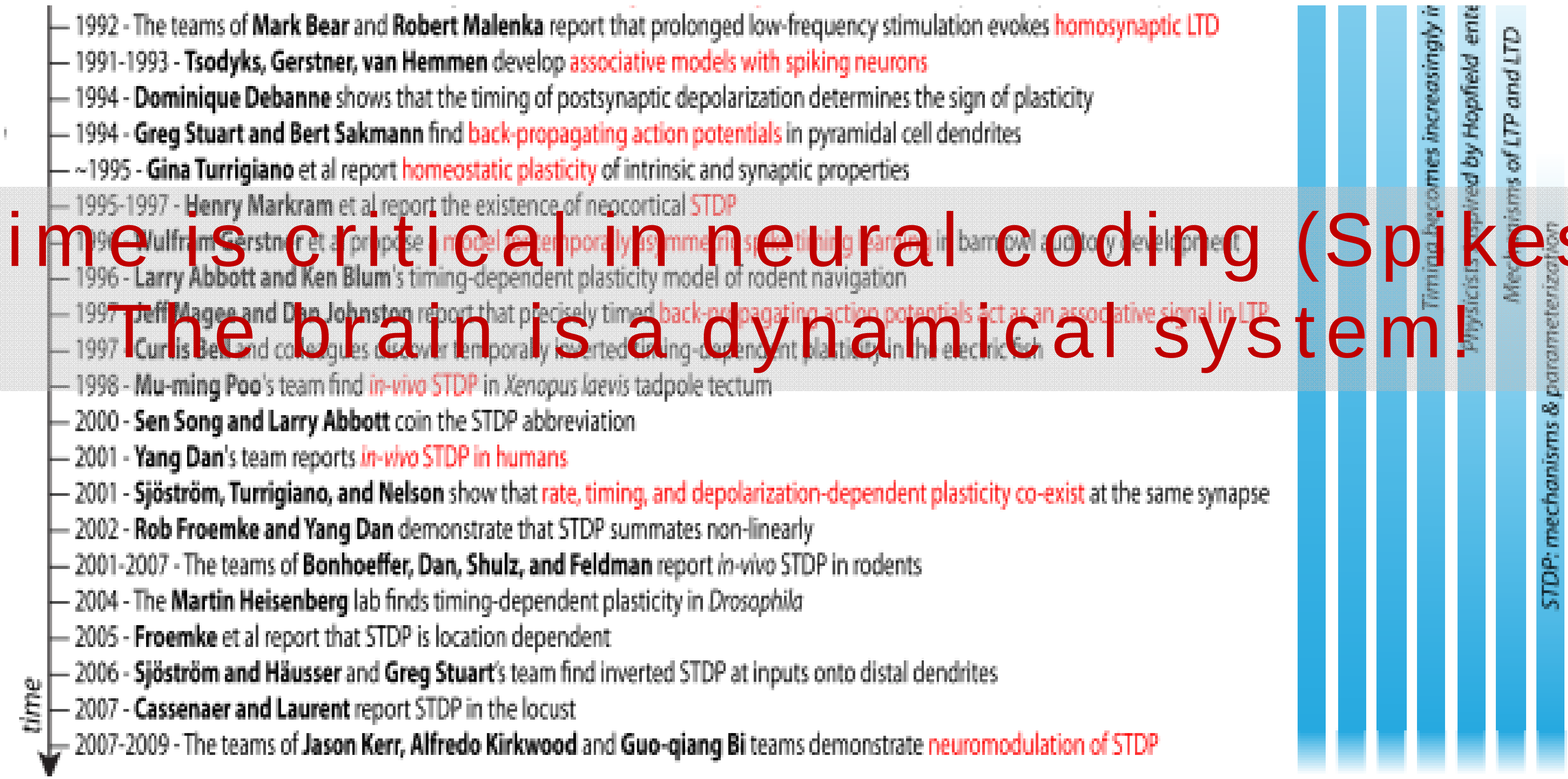
- Philips : L-Neuro
  - 1st Gen 16PEs 26 MCps
  - 2nd Gen 12 PEs 720 MCps
- + Intel (ETANN), AT&T (Anna), Hitachi (WSI), NEC, Thomson (now THALES), etc…
- CEA MIND machine
  - Hybrid analog/digital: MIND-128
  - Fully digital: MIND-1024





However During the 1990's

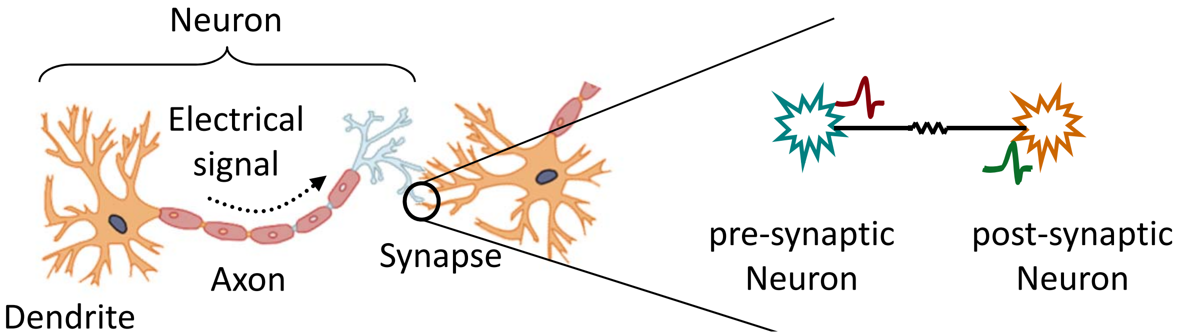
- Progresses in Neuroscience demonstrated the weaknesses of the perceptron approach and introduced LTP/LTD and STDP



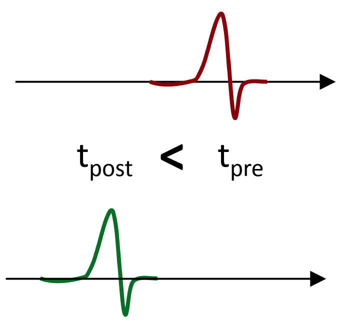
Time is critical in neural coding (Spikes)
The brain is a dynamical system!

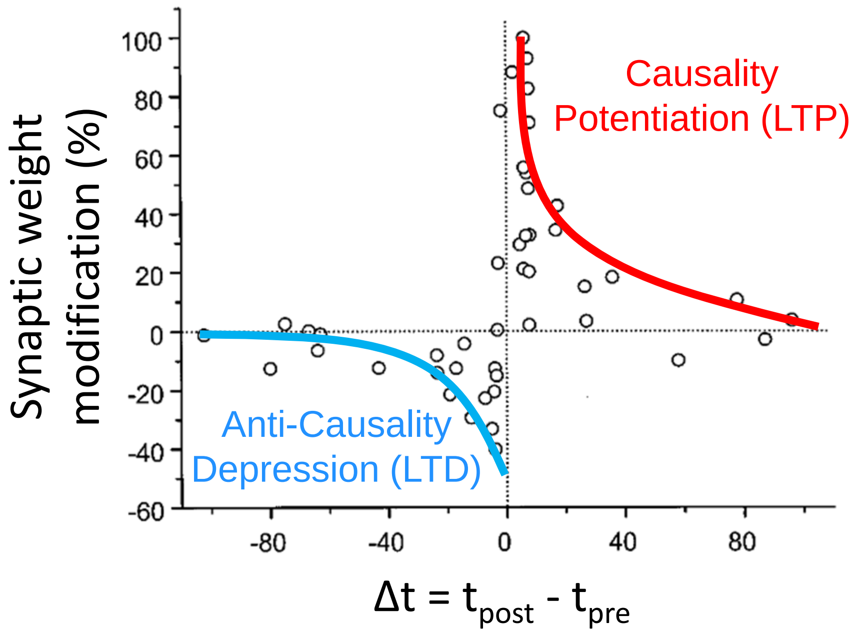
from Markram et al. "A history of spike-timing-dependent plasticity," in *Frontiers in Synaptic neuroscience*, Vol 3, August 2011

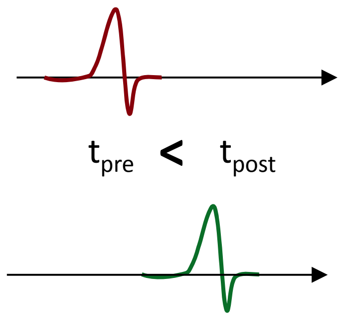
Learning from neurosciencex: a STDP Primer



STDP = correlation detector
➔ Possible learning model of the mind

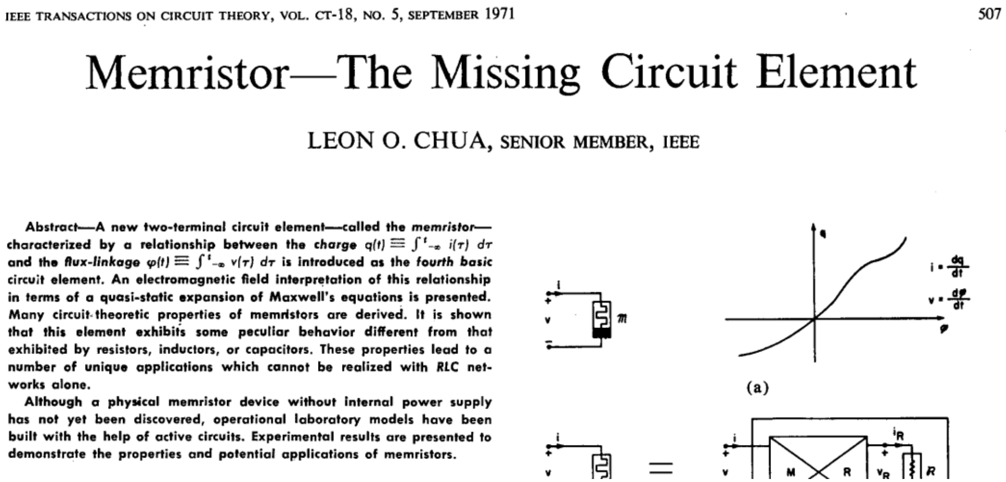






A brief memri-story

- Introduced by Leon Chua, 1971



IEEE TRANSACTIONS ON CIRCUIT THEORY, VOL. CT-18, NO. 5, SEPTEMBER 1971 507

Memristor—The Missing Circuit Element

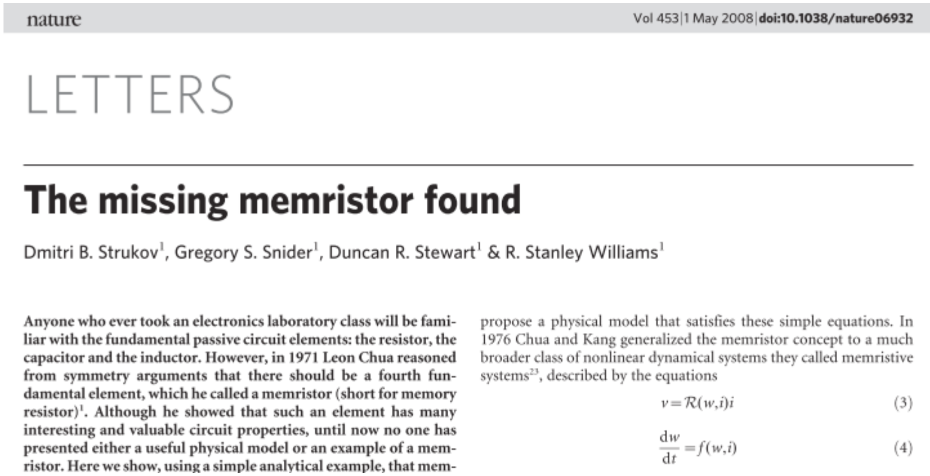
LEON O. CHUA, SENIOR MEMBER, IEEE

Abstract—A new two-terminal circuit element—called the *memristor*—characterized by a relationship between the *charge* $q(t) \equiv \int_{-\infty}^{t} i(\tau)\,d\tau$ and the *flux-linkage* $\varphi(t) \equiv \int_{-\infty}^{t} v(\tau)\,d\tau$ is introduced as the *fourth basic* circuit element. An electromagnetic field interpretation of this relationship in terms of a quasi-static expansion of Maxwell's equations is presented. Many circuit-theoretic properties of memristors are derived. It is shown that this element exhibits some peculiar behavior different from that exhibited by resistors, inductors, or capacitors. These properties lead to a number of unique applications which cannot be realized with *RLC* networks alone.

Although a physical memristor device without internal power supply has not yet been discovered, operational laboratory models have been built with the help of active circuits. Experimental results are presented to demonstrate the properties and potential applications of memristors.

- Revisited by Strukov et al., 2008



nature Vol 453|1 May 2008|doi:10.1038/nature06932

LETTERS

The missing memristor found

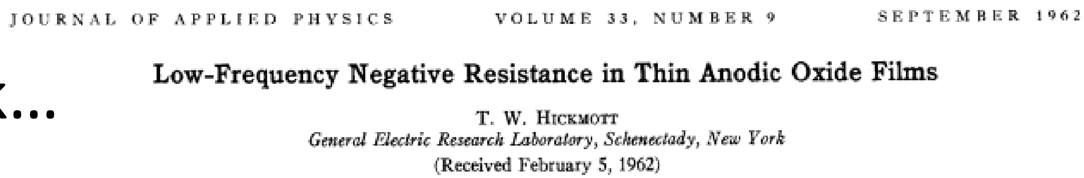
Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

Anyone who ever took an electronics laboratory class will be familiar with the fundamental passive circuit elements: the resistor, the capacitor and the inductor. However, in 1971 Leon Chua reasoned from symmetry arguments that there should be a fourth fundamental element, which he called a memristor (short for memory resistor)[1]. Although he showed that such an element has many interesting and valuable circuit properties, until now no one has presented either a useful physical model or an example of a memristor. Here we show, using a simple analytical example, that memristive systems propose a physical model that satisfies these simple equations. In 1976 Chua and Kang generalized the memristor concept to a much broader class of nonlinear dynamical systems they called memristive systems[23], described by the equations

$$v = \mathcal{R}(w,i)i \qquad (3)$$

$$\frac{dw}{dt} = f(w,i) \qquad (4)$$

- Spotted way back…



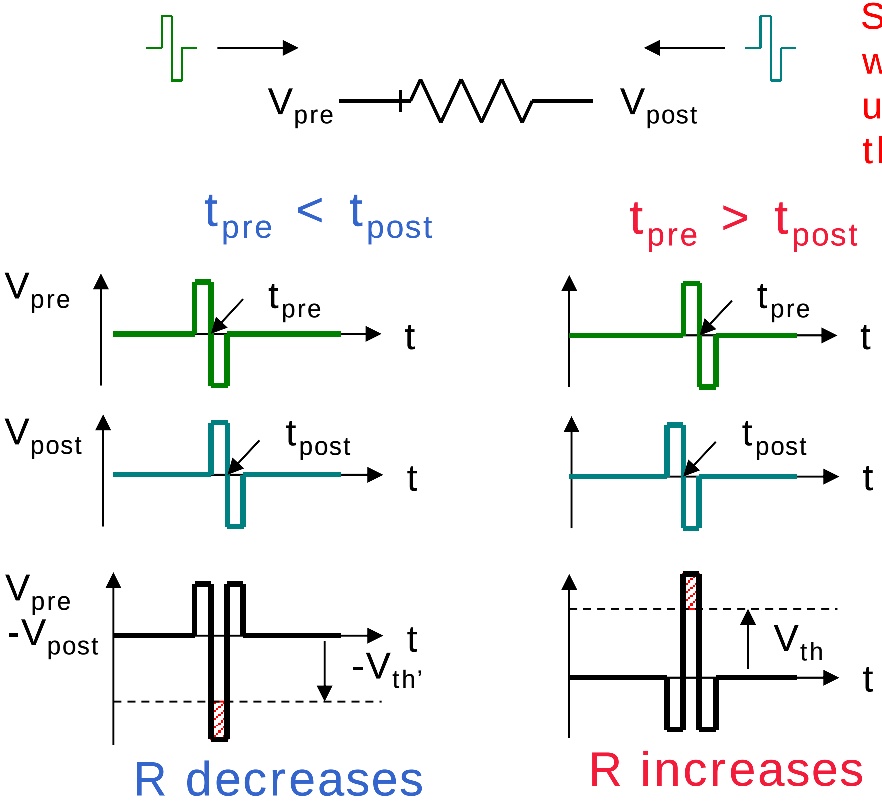
JOURNAL OF APPLIED PHYSICS VOLUME 33, NUMBER 9 SEPTEMBER 1962

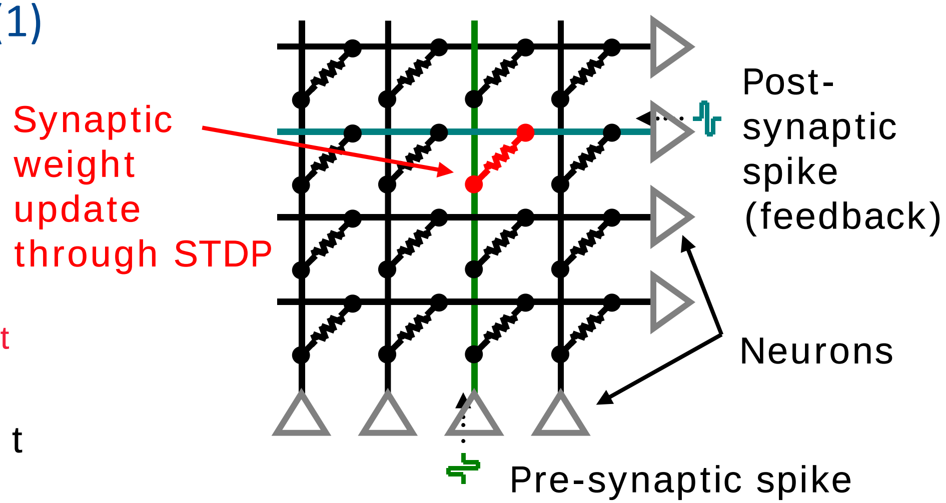
Low-Frequency Negative Resistance in Thin Anodic Oxide Films

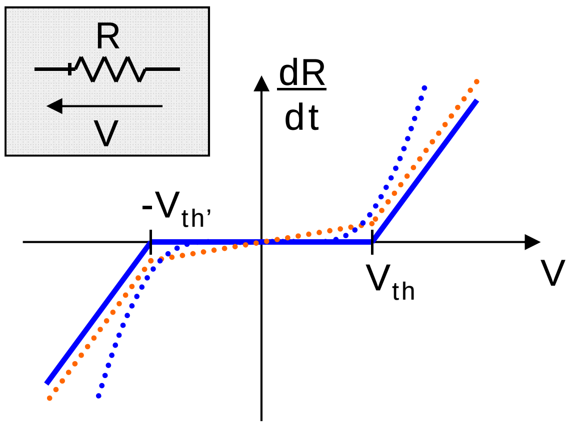
T. W. Hickmott
General Electric Research Laboratory, Schenectady, New York
(Received February 5, 1962)

The meeting of Memristors & STDP

First Proposed by Snider(1)





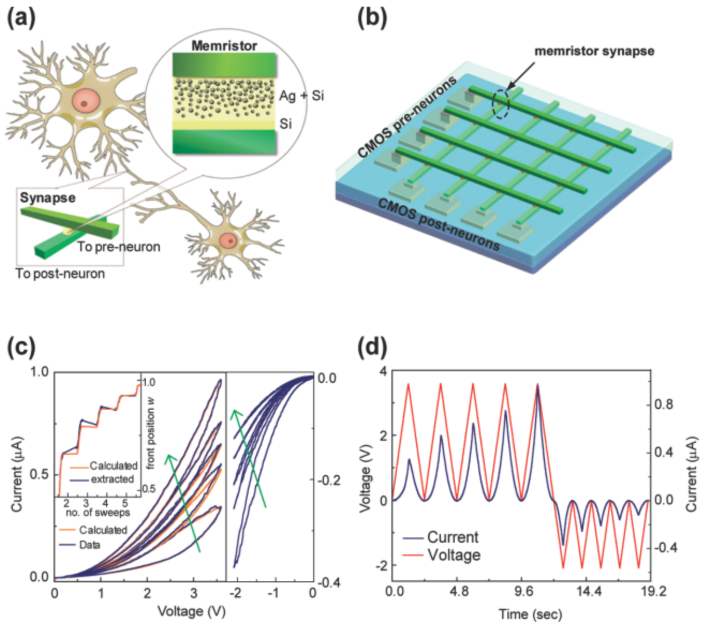


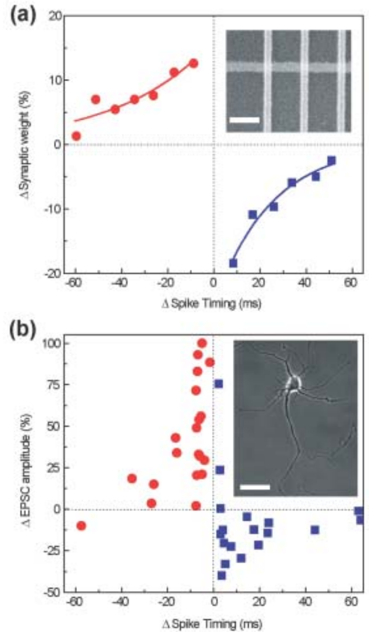
1. G. Snider, *Nanoscale Architectures*, 2008
2. B. Linares-Barranco and T. Serrano-Gotarredona, *Nature Precedings*, 2009

STDP experimental demonstration

U. Michigan, Lu group demonstration

[1] Jo, S.H. et al. Nanoscale Memristor Device as Synapse in Neuromorphic Systems. *Nano Letters* (2010).



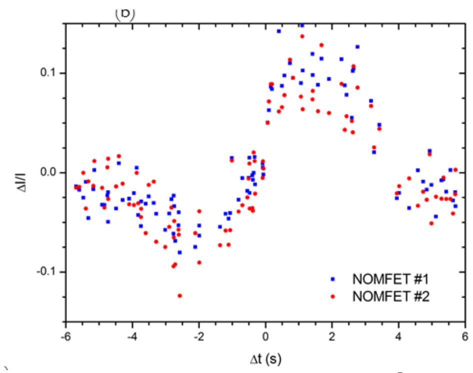


Demonstration on PC memory by Wong group, Stanford

D. Kuzum et al, "Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing," *Nano Letters*, 2011

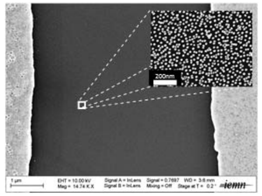
Demonstrated on NOMFET devices

F. Alibart et al. "A Memristive Nanoparticle/Organic Hybrid Synapstor for Neuroinspired Computing,"
Advanced Functional Materials, vol. 22, no. 3, pp. 609–616, 2012.

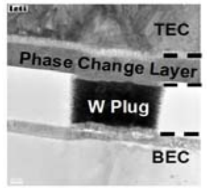


The realm of memristive technologies

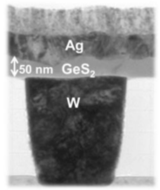
- **Metal Oxide devices (OxRAM)**
  - Bipolar
  - A wide variety of materials: TiO2, HfO2, VO2, …..

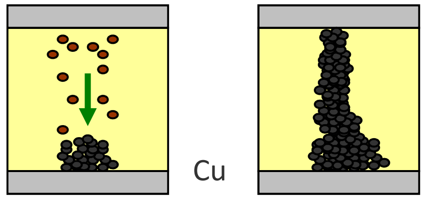


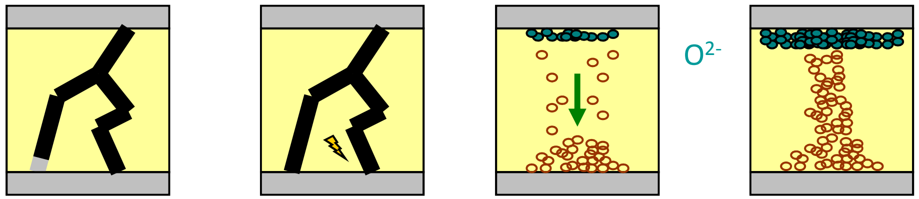
- **Nanoparticle Organic Memory FET(NOMFET)**
  - Transistor like, Low retention time



- **Phase Change Memory (PCM)**
  - Unipolar -> cumulative in 'SET' direction only
  - "High" programming voltage
- **Conductive Bridge memory(CBRAM)**
  - Binary
  - Only set with current compliance is Multi-level

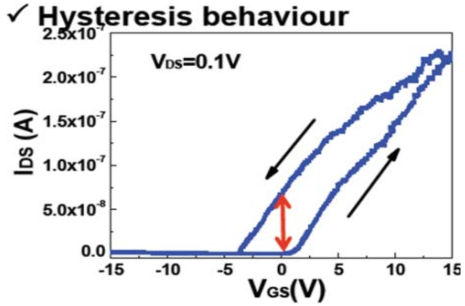


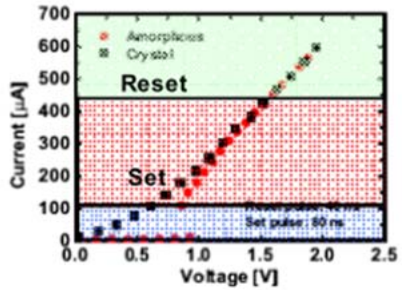




Memristive Device Properties

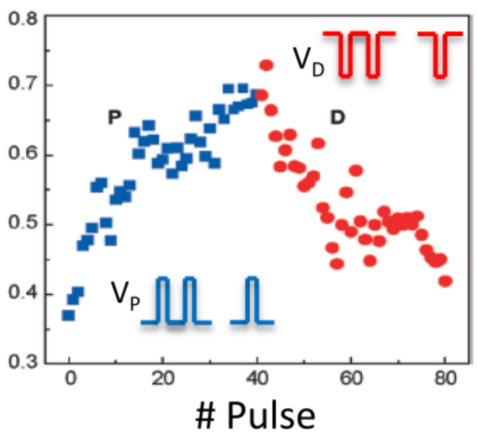
- Polarity
  - Bipolar devices: OxRAM
  - Unipolar devices: PC RAM
  - Bipolar/binary : CBRAM



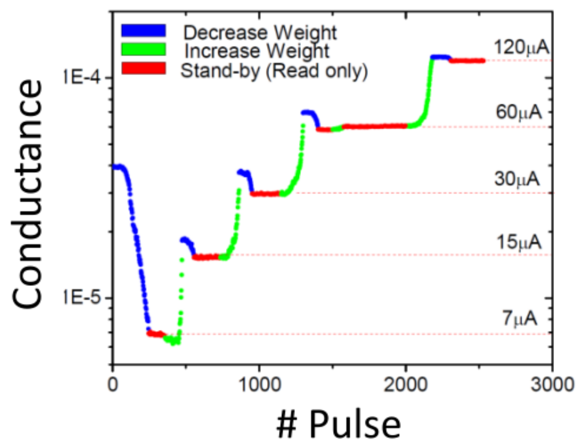


- Basic properties of synapse-like candidate
  - Cumulativity -> keeps NV memory of state
  - Either multi-level-ability or stochasticity

Cumulative effect

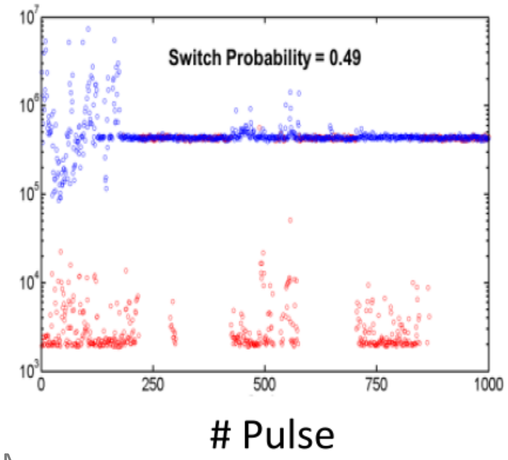


Multi-level



Wei Lu

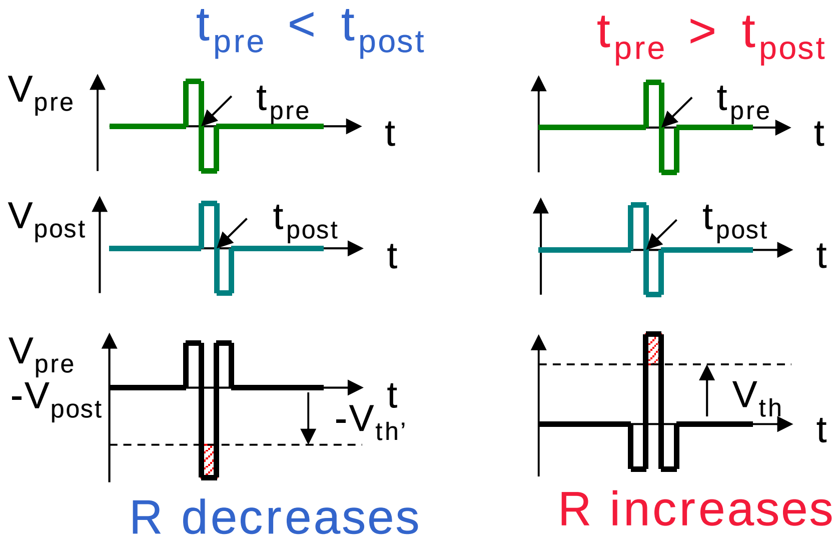
Stochastic behavior

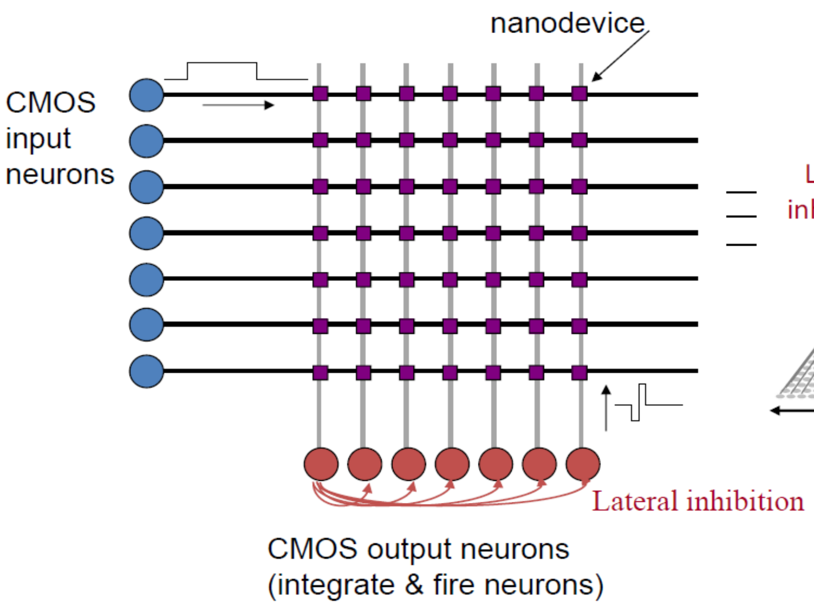


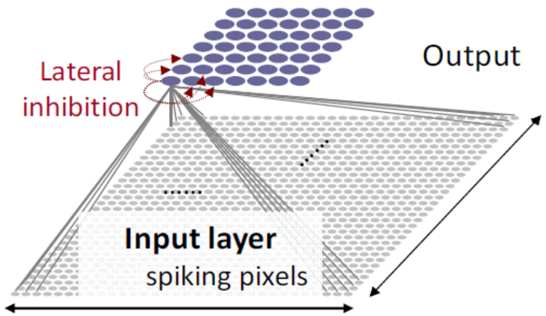
Designing for bipolar devices

- The original idea from Snider

- Crossbar style design
  - With or without access To
  - Sneak path issue
  - Crossbar size issue

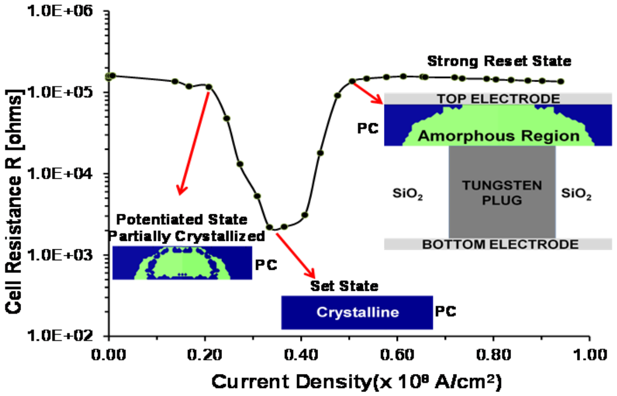


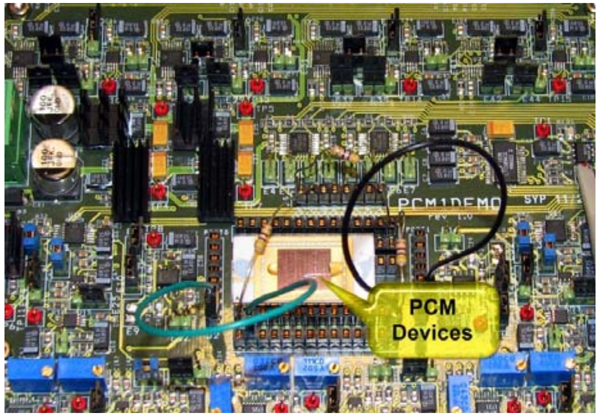




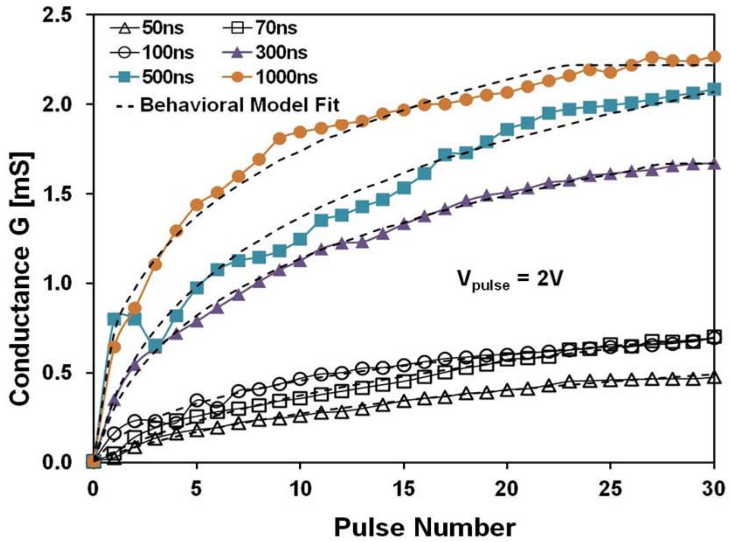
Designing for unipolar devices

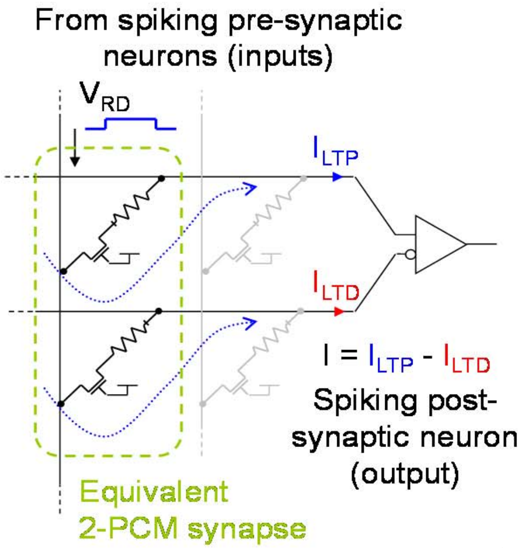
- PCM is typically unipolar due to its physics





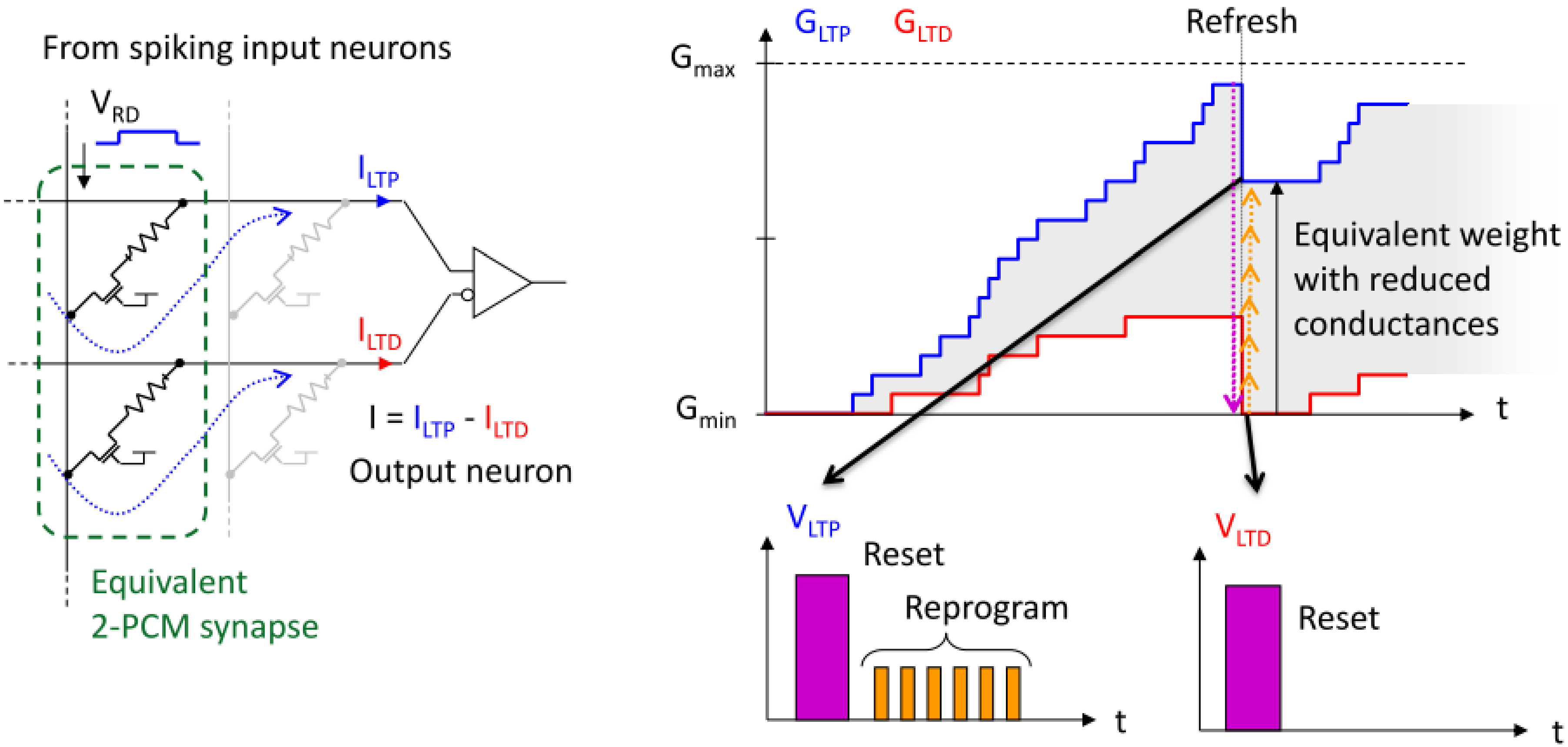
- It requires a specific 2-PCM circuits





Designing for unipolar devices

- Emulate an "ideal" synapse with PCM
  - Use 2 PCM both in gradual crystallization
  - Implement a refresh protocol to avoid saturation



CBRAM: a binary device

- CBRAM is a typical binary device
- Bipolar
  - +Vset = +1,5 V = SET
    - Creation of a filament
  - -Vreset = -1,5V = RESET
    - Destruction of the filament
- Binary (w/o I compliance)
  - Low resistance state (≈4,5k Ω)
  - High resistance state (≈10M Ω)

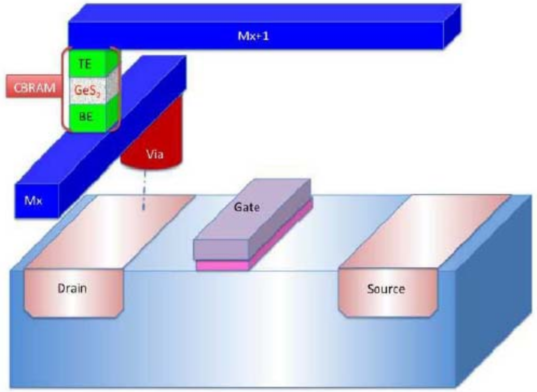
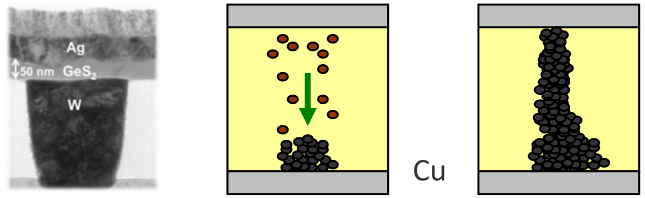


Fig. 1: CBRAM device in BEOL. The CBRAM consists in Metal - Insulator - Metal (MIM) structure with Transition Metal Oxide (TMO) sandwiched between TE and BE contacts. It co-habitats with a via between BEOL metal levels. Here it is in BEOL integrated with Front End Of Line (FEOL) select transistor in a standard CMOS process flow.

Synapses are naturally multi-level,
how can binary devices be used as synapses?

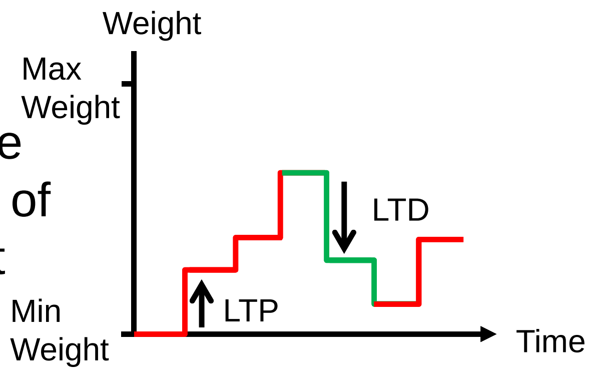


[1] Reyboz, M.; Onkaraiah, S.; Palma, G.; Vianello, E.; Perniola, L., "Compact model of a CBRAM cell in Verilog-A," *Non-Volatile Memory Technology Symposium (NVMTS), 2012*

Designing for binary devices

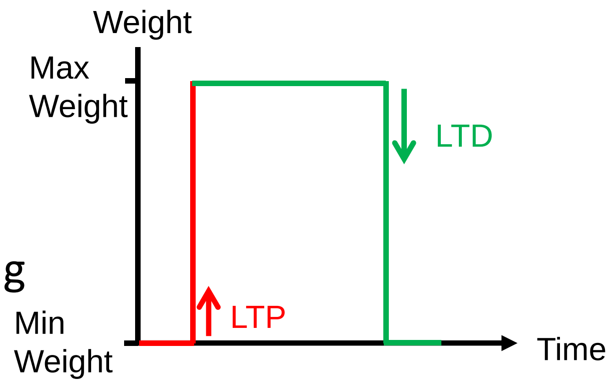
- Possible synaptic implementation
  - Analog device

Progressive modification of the weight



  - Binary device

For a binary device, the weight reflects the last learning operation !



  - Stochasticity !

By using probabilistic programming, the synapse will reflect the overall result on a long term learning process

- Intrinsic : Weak programming pulse

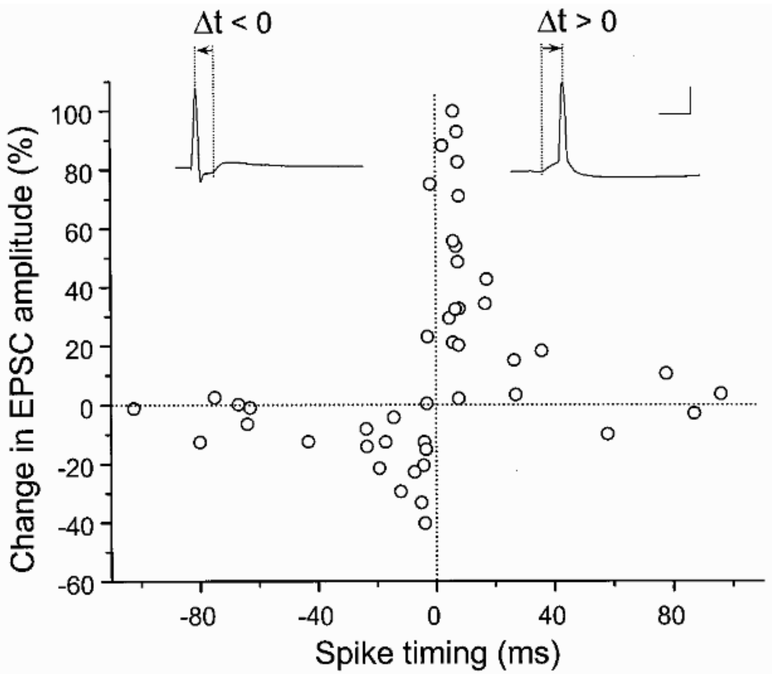
  A weak pulse has a given probability to switch the device

- Extrinsic: Pseudo-Random number generator

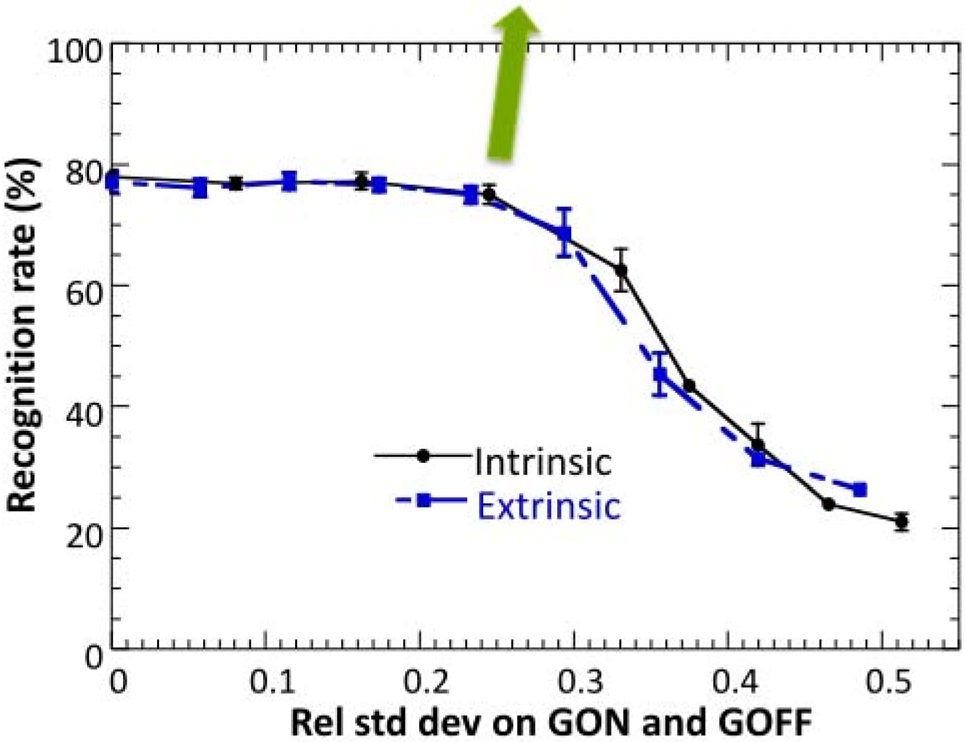
  We control the probability to send a pulse

Stochastic STDP

- Stochastic learning
  + Monte Carlo simulation

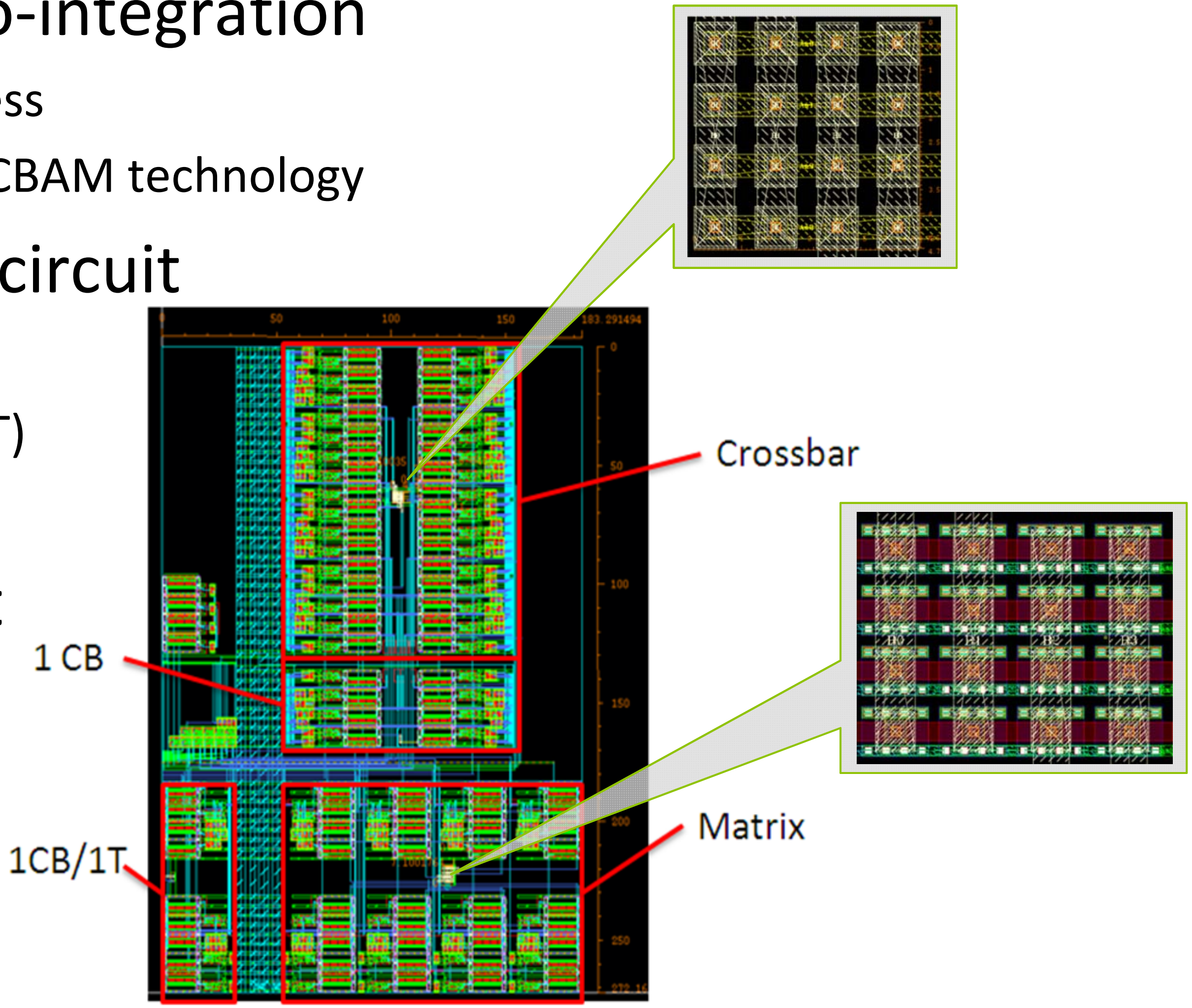


Stochastic STDP learning rule with binary memory devices



A CBRAM test chip

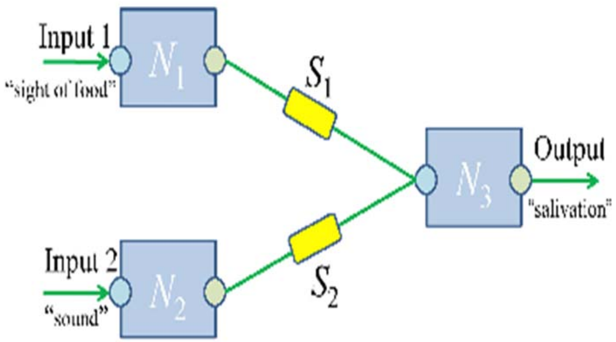
- CMOS/CBRAM Co-integration
  - 130 nm CMOS process
  - Industrially mature CBAM technology
- Proof of concept circuit
  - 4*4 Crossbar (1CB)
  - 4*4 Matrix (1CB – 1T)
- Chip is under test



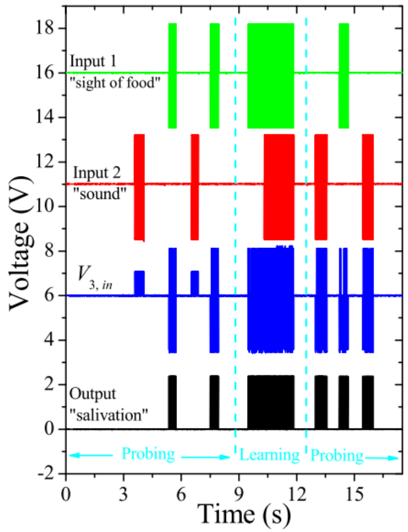
Crossbar : 4.72 µm * 4.72 µm
Matrix : 5.15 µm * 7.1 µm

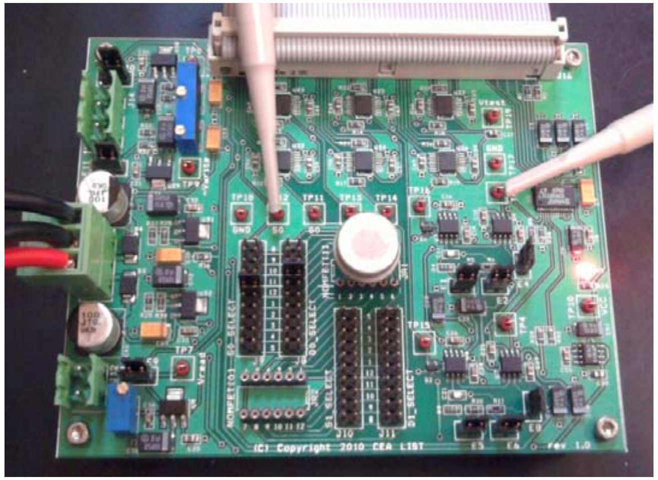
- What kind of applications for such circuits?
- Can they really learn?
- Some interesting results…

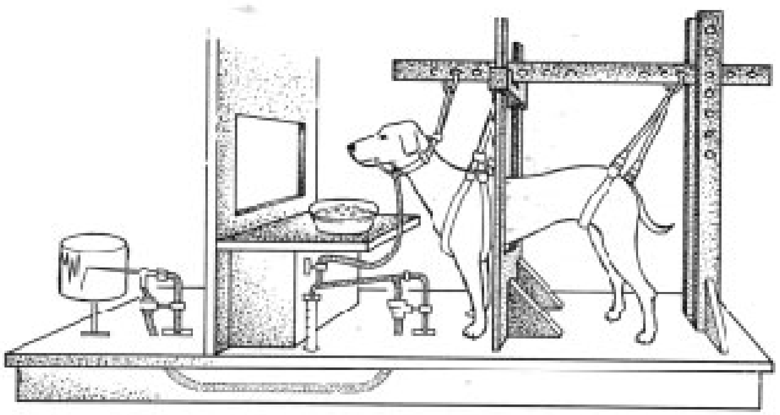
A dog with 2 synapses!

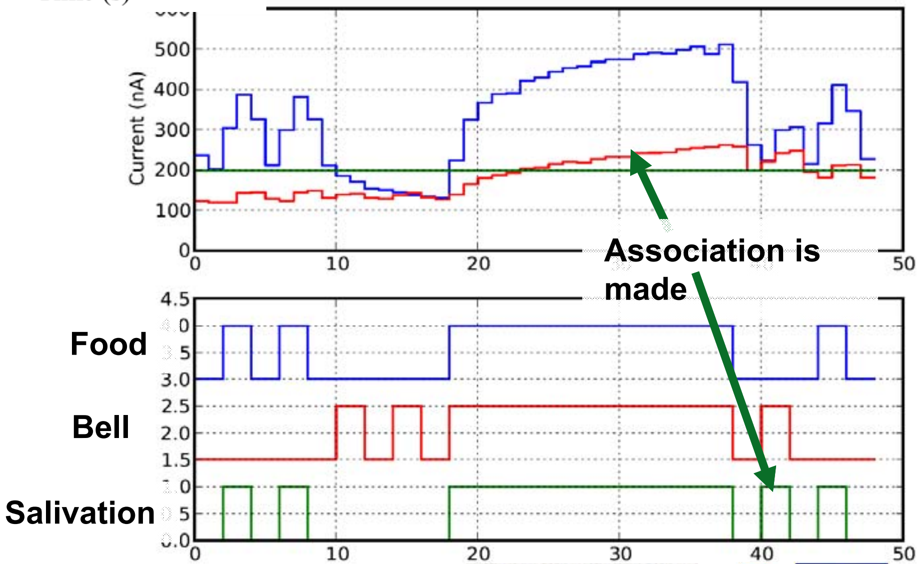


Experimental setup for a Pavlovian associative memory based on memristive devices as proposed by Di Ventra et col.[2]



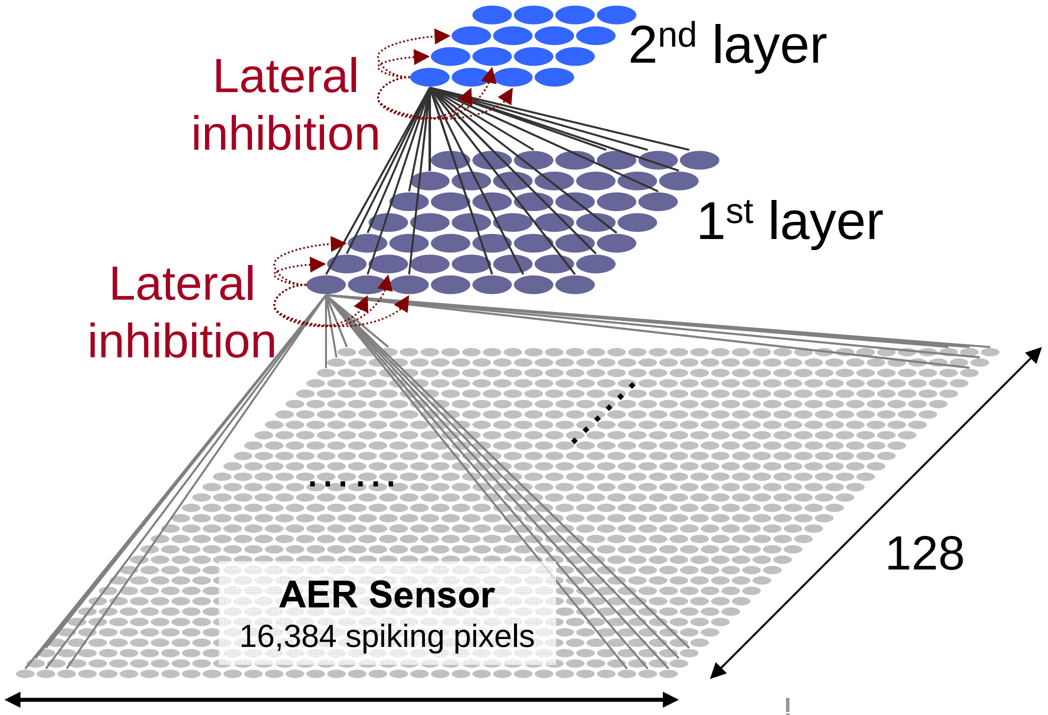


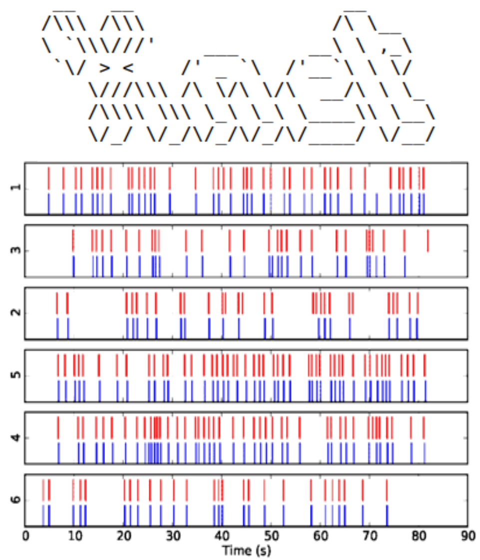




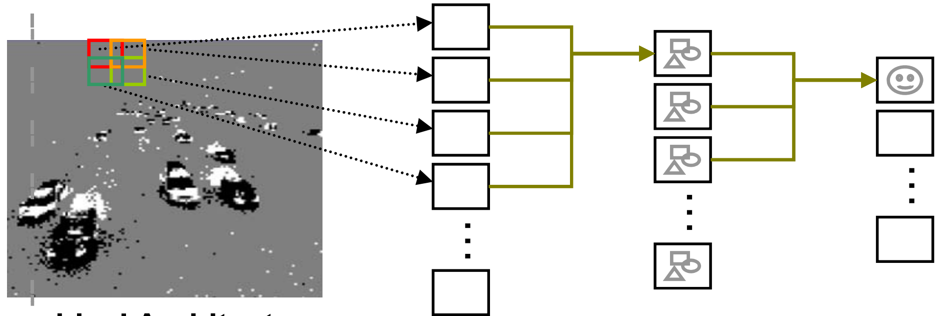
[1] O. Bichler, W. Zhao, F. Alibart, S. Pleutin, S. Lenfant, D. Vuillaume, C. Gamrat, "Pavlov's Dog Associative Learning Demonstrated on Synaptic-like Organic Transistors", Neural Computation, 2012
[2] Pershin, Y.V. & Di Ventra, M. "Experimental demonstration of associative memory with memristive neural networks." Arxiv *0905.2935* (2009).

A pretty realistic application example





Two-layers system
~ 2 million devices with STDP

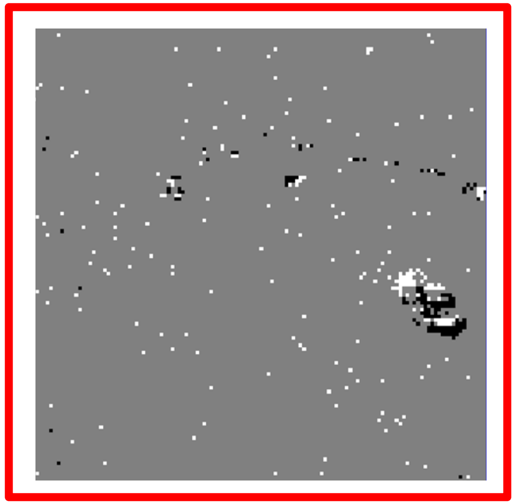


Hierarchical Architecture Proposal

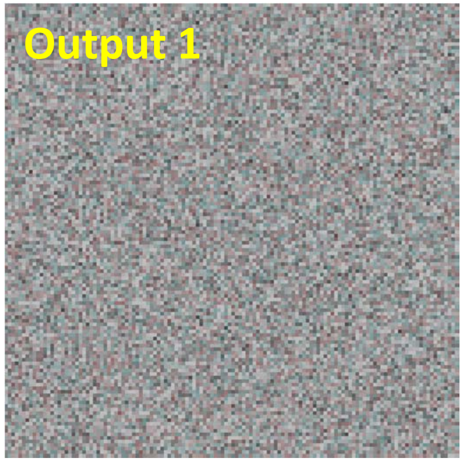
O. Bichler, D. Querlioz, S. J. Thorpe, J.-P. Bourgoin and C. Gamrat, *"Unsupervised Features Extraction from Asynchronous Silicon Retina through Spike-Timing-Dependent Plasticity"*, International Joint Conference on Neural Networks IJCNN August 2011

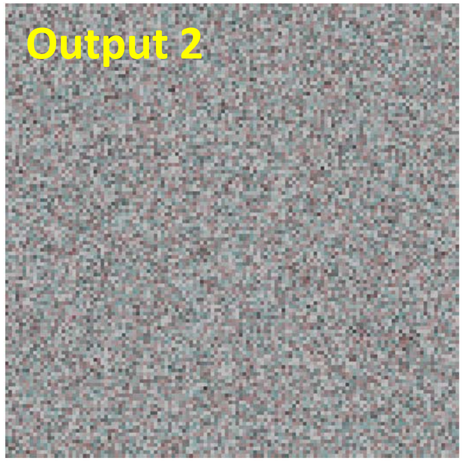
Weights Evolution During Learning

Recorded stimuli



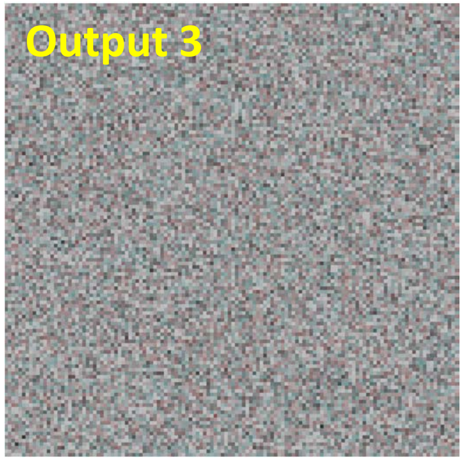
Synaptic maps for 4 neurons on the first layer

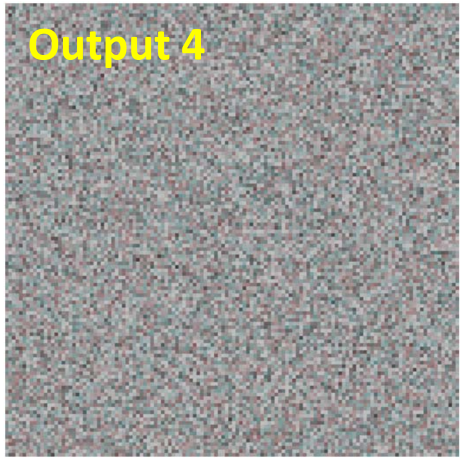




Lane 2

Lane 4



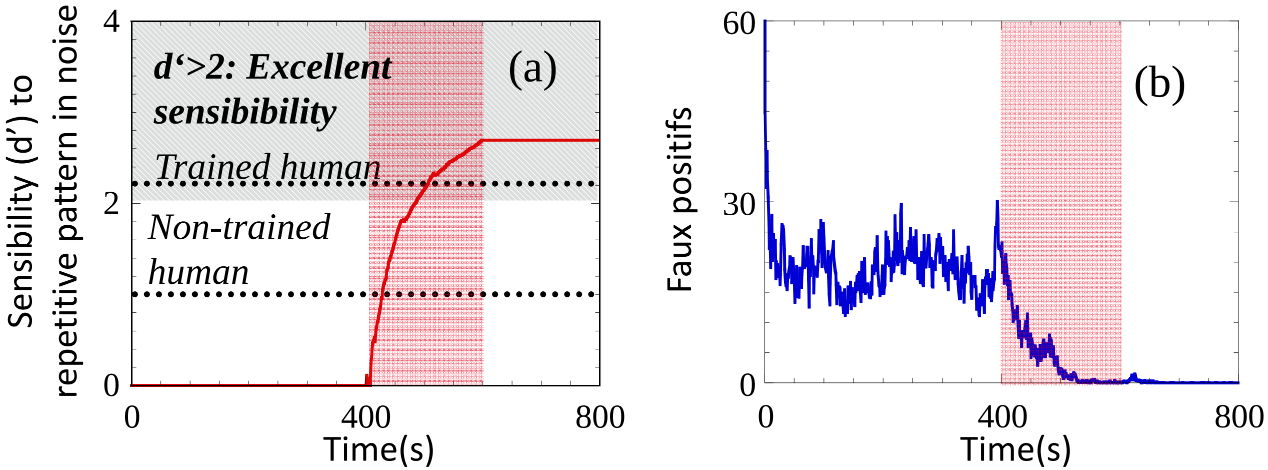


Lane 5

Lane 1

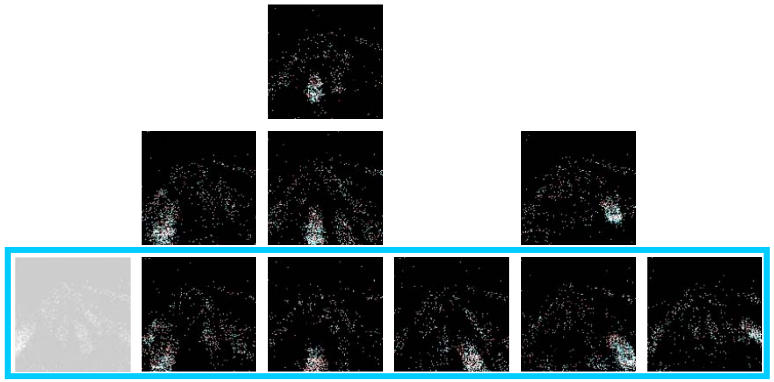
Learning with stochastic STDP on CBRAM

- Learning of auditory pattern (3 CBRAM/synapse)



AER EAR2 silicon cochlea
Shih-Chii Liu and Tobi Delbruck

- Learning of trajectory (1 CBRAM/synapse)



1st lane 2nd lane 3rd lane 4th lane 5th lane 6th lane

- Pattern classification

Recognition rate MNIST database:
72% with 5 CBRAM/synapse

Results : D. Querlioz (IEF)

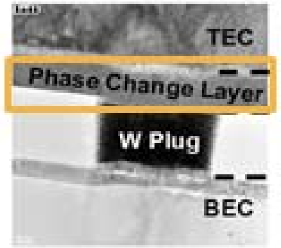
Wrap up

Memristive technologies

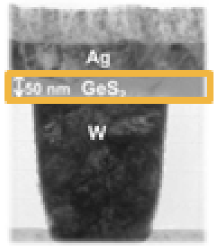
Synaptic-like devices

PCM

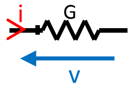
RRAM (CBRAM/OXRAM)



ST/LETI



ALTIS/LETI

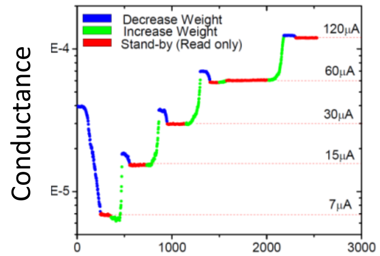


$i = G.v$

$$\frac{dG}{dt} = f(v, G)$$

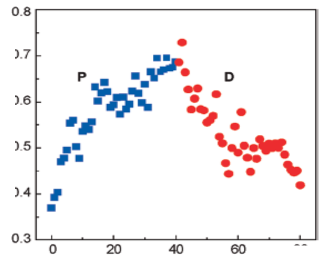
f() non linear

Multi-level



F. Alibart

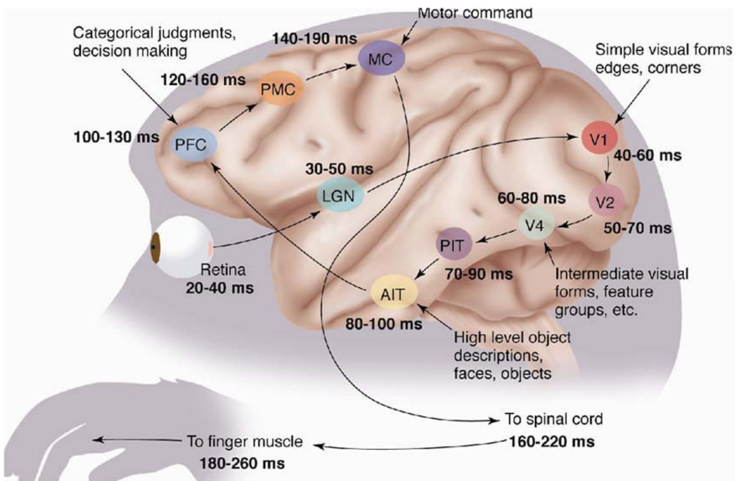
Cumulativity



Wei Lu

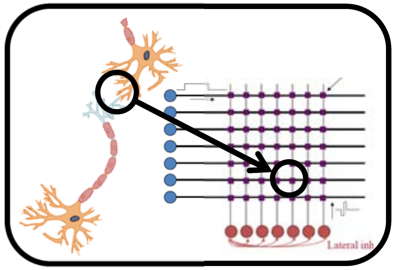
Pulse base coding

(Human visual system)



S.J. Thorpe

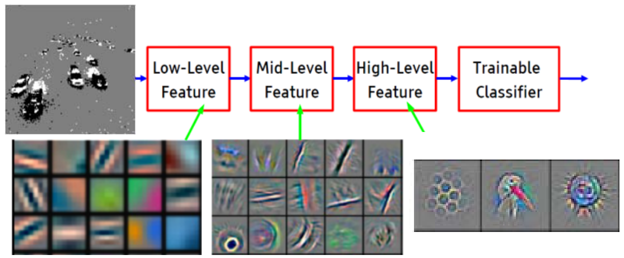
Circuit Design

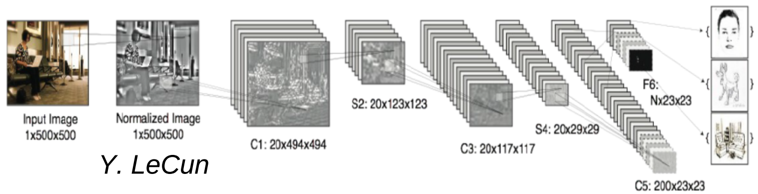


Embedded cognitive functions

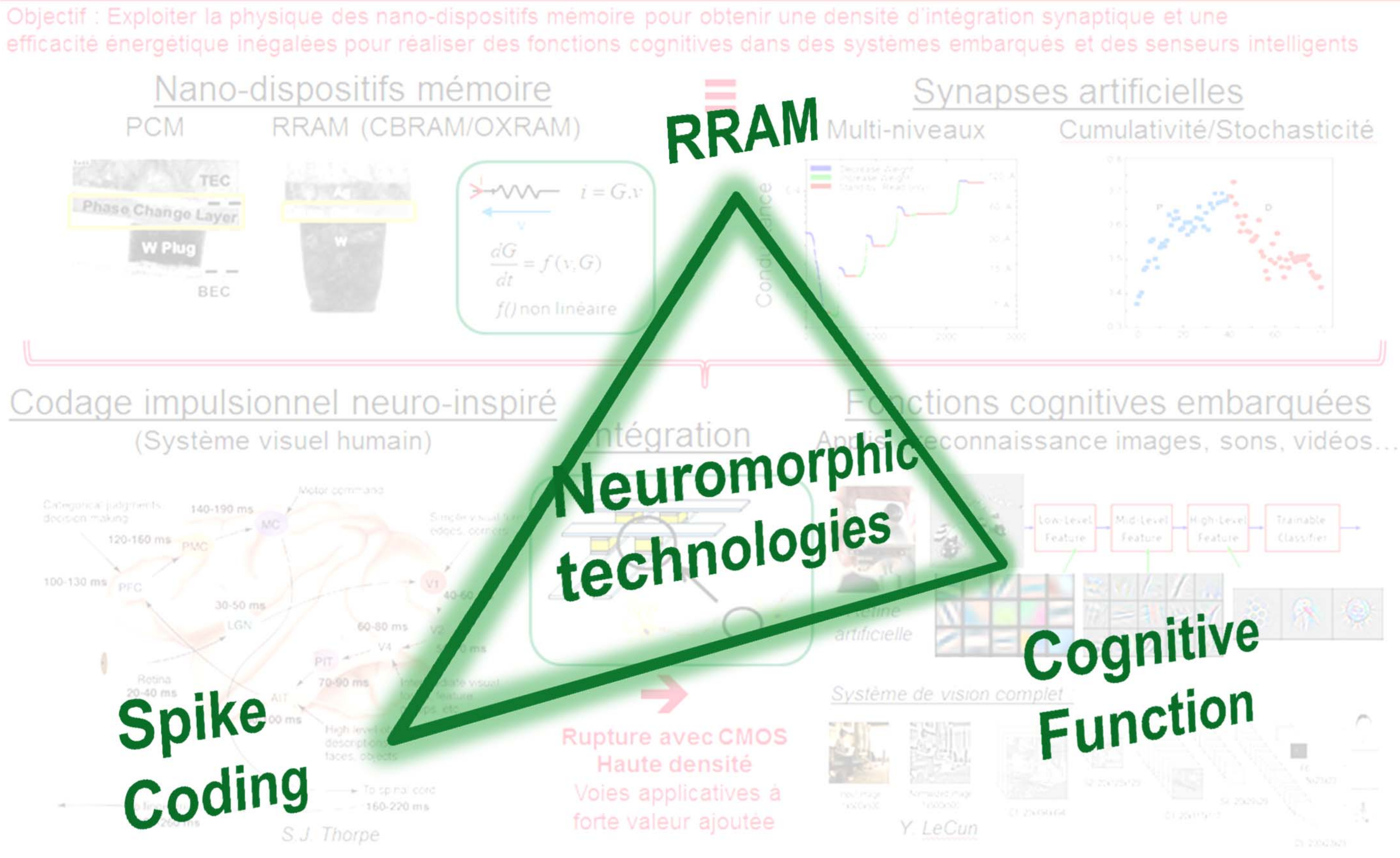
Apps : image, audio, natural data sensing

Artificial retina





Y. LeCun


Objectif : Exploiter la physique des nano-dispositifs mémoire pour obtenir une densité d'intégration synaptique et une efficacité énergétique inégalées pour réaliser des fonctions cognitives dans des systèmes embarqués et des senseurs intelligents
Nano-dispositifs mémoire
PCM
RRAM (CBRAM/OXRAM)
TEC
Phase Change Layer
W Plug
BEC
W
i = G.v
dG/dt = f(v,G)
f() non linéaire
Synapses artificielles
Multi-niveaux
Cumulativité/Stochasticité
Codage impulsionnel neuro-inspiré
(Système visuel humain)
Intégration
Fonctions cognitives embarquées
Applis : reconnaissance images, sons, vidéos…
Low-Level Feature
Mid-Level Feature
High-Level Feature
Trainable Classifier
Rétine artificielle
Système de vision complet
Rupture avec CMOS
Haute densité
Voies applicatives à forte valeur ajoutée
S.J. Thorpe
Y. LeCun
RRAM
Neuromorphic technologies
Spike Coding
Cognitive Function

Take away message

- For each families of memristive devices there exist design solutions
  - Probabilistic equivalent of STDP for binary devices are possible
- A new Neuro-engineering approach combining
  - A spike based coding scheme
  - Unsupervised learning rule based on STDP
  - An implementation technology based on memristive devices
    - Implementing STDP learning right from its physics
- Potential
  - Memristive devices can also be exploited as std NV memories -> ideas…
  - A promising way for **low power embedded cognitive functions**
- Still a lot of work ahead
  - Architecture and design questions: Xbar vs Matrix?
  - Which technology will be the right one?

Last, but certainly not least….

Many thanks to those without whom this would not be

@ our end
- David Roclin,
- Olivier Bichler

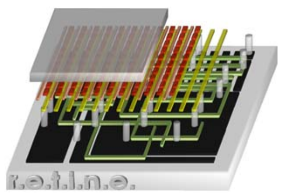
@ LETI
- Barbara de Salvo,
- Manan Suri

@ CNRS, IEMN, Lille
- Dominique Vuillaume
- Fabien Allibart

@ Université Paris-Sud
- Jacques Olivier Klein
- Damien Querlioz
- Weisheng Zhao

@ CNRS, Toulouse
- Simon Thorpe

Our Funding Sources :
- **FP7 Framework**
- **Agence Nationale de la Recherche**
- **Université Paris-Saclay**



Thank you!

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Power Estimation with PCM Synapstors (Car Detection App)

$$E_{\text{Synaptic learning}} = E_{\text{RESET total}} + E_{\text{SET total}}$$

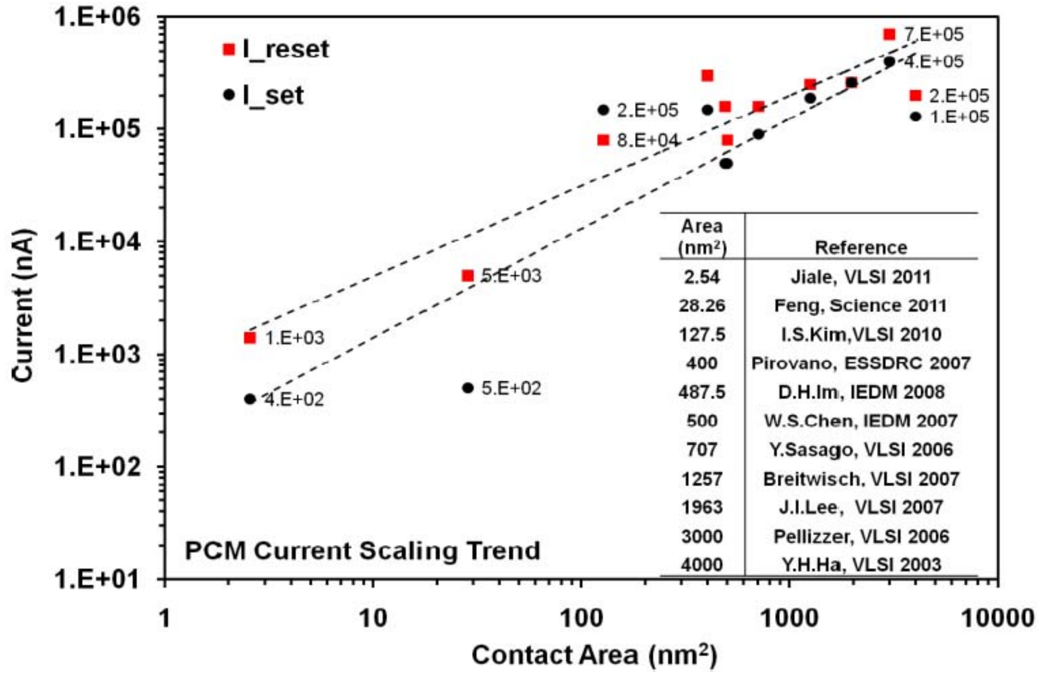
$$P_{\text{System}} = E_{\text{Synaptic learning}} / \text{Learning time}$$

GST Devices

$E_{\text{reset/spike}} =$ 1552 pJ

$E_{\text{set/spike}} =$ 121 pJ

$P_{\text{system}} =$ 112 µW



P_{System} could go as low as 20 nW !!

- *M. Suri et al. "Phase Change Memory as Synapse for Ultra-Dense Neuromorphic Systems: Application to Complex visual pattern extraction", IEDM 2011, Washington, December 2011*

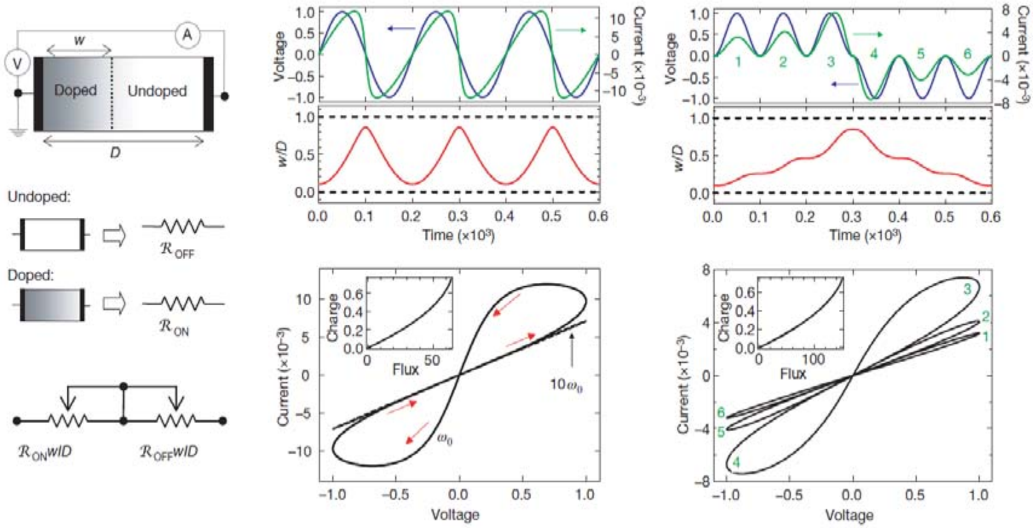
Memristive Devices Principle

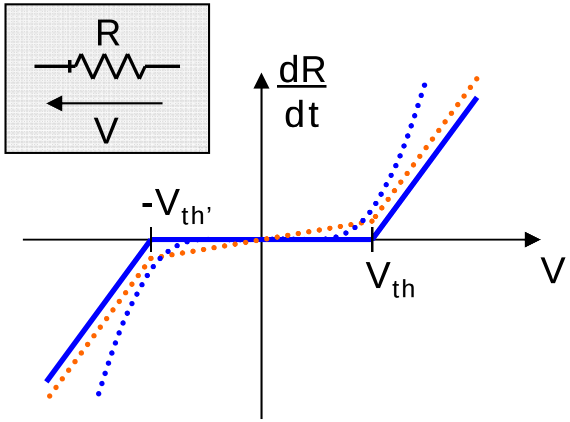
Important steps

- First theoretical study[1]

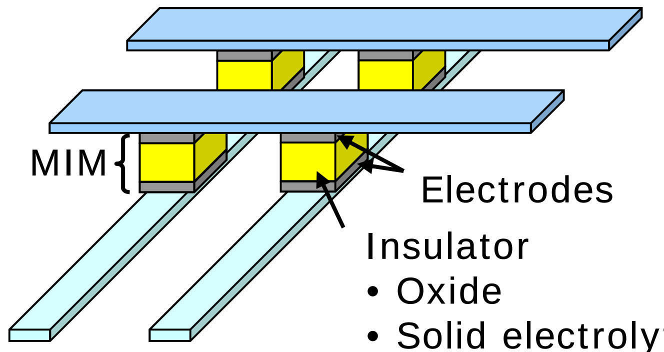
$$v = R(x,i).i \qquad \frac{dx}{dt} = f(x,i)$$

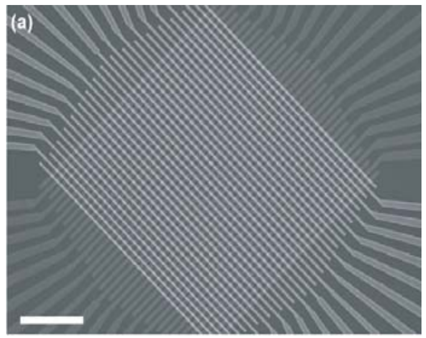
- First link between a physical device and the theory[2]
- STDP learning





Nonlinear characteristic required for STDP!





Crossbar
(University of Michigan)

[1] L. Chua and S. Kang, *Proceedings of the IEEE*, 1976
[2] D. Strukov et al., *Nature*, 2008